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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,920	01/24/2002	Mark Roh	010450	3753

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EXAMINER	
CHO, HONG SOL	
ART UNIT	PAPER NUMBER
2616	

NOTIFICATION DATE	DELIVERY MODE
10/05/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/056,920	ROH ET AL.	
	Examiner	Art Unit	
	Hong Cho	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5, 9-21, 23, 25, 27-31, 33-46, 49-56, 59-71, 73, 75, 77-81 and 83-86 are* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-21,23,41-46,49,50,64-71 and 73* is/are allowed.

6)☒ Claim(s) *1-6,9-13,25,27-31,33-37,51-56,59-63,75,77-81 and 83-86* is/are rejected.

7)☒ Claim(s) *38-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to the amendment filed on 08/17/2007. Claims 7, 8, 22, 24, 26, 32, 47, 48, 57, 58, 72, 74, 76 and 82 have been cancelled. Claims 1-5, 9-21, 23, 25, 27-31, 33-46, 49-56, 59-71, 73, 75, 77-81 and 83-86 are pending in the instant application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 9-13, 51-55 and 59-63, are rejected under 35 U.S.C. 103(a) as being unpatentable over Brunner et al (U.S 6567462), hereinafter referred to as Brunner, in view of Yamada et al (US 5822364), hereinafter referred to as Yamada.

Re claims 1 and 51, Brunner discloses obtaining pilot spreading codes (*time offset information*) from received radio signal (*a first signal*) (*searching for time offset information signal in a first signal*, column 2, lines 44-48). Brunner discloses correlating a received signal (*a first signal*) with a user data spreading codes (*a second signal*)

(*producing a plurality of first correlated values from a portion of the first signal and a second signal*, column 10, lines 17-22), outputting correlated samples (*a plurality of first correlated values)* to a discrete Fourier transformer (*transforming the first correlated values into a plurality of second correlation values related to a frequency content of the first correlation values*, column 12, lines 34-38) and recovering data symbols by using the outputs (*second correlated values)* of the discrete Fourier transformer (*searching for time offset information by evaluating the second correlation values*, column 9, lines 58-67). Brunner fails to disclose coherently combining different portions of the product values to produce a plurality of coherent sums each comprising one of the first correlation values. Yamada discloses adders producing three coherent sums (figure 2, element 26; column 6, lines 21-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Brunner to implement a multiplier and adders of the Yamada for the benefit of preventing the received signal from becoming degraded.

Re claims 2 and 52, Brunner discloses the time offset information corresponding to a pilot signal (figure 3b, element 30).

Re claims 3 and 53, Brunner discloses receiving a spread pilot signal (*a pilot signal spread by a code*) and correlating with a user data spreading codes (*a second signal comprising a replica of the code*, column 7, lines 64-66).

Re claims 4 and 54, Brunner inherently discloses the code comprising a pseudo-random code.

Re claims 5 and 55, Brunner discloses the first and second signal comprising a plurality of chips (figure 3b).

Re claims 9 and 59, Brunner and Yamada disclose producing three coherent sums by combining three delayed signals with optimum weights, but fail to disclose producing 96 product values from the multiplication of the first signal portion with the second signal. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Brunner and Yamada to produce 96 products for the benefit of preventing the received signal from becoming degraded.

Re claims 10 and 60, Brunner and Yamada disclose producing three coherent sums by combining three delayed signals with optimum weights, but fail to disclose combining three different product value portions each comprising 32 product values. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Brunner and Yamada to combine three product value portions for the benefit of preventing the received signal from becoming degraded.

Re claims 11-13 and 61-63, Brunner discloses the frequency device being a discrete Fourier transformer or a fast transformer (column 4, lines 24-23).

Claims 25, 27-31, 33, 37, 75, 77-81, 83 and 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al (U.S 6414985), hereinafter referred to as Furukawa, in view of Yamada.

Re claims 25, 37, 75, and 86, Furukawa discloses a detection circuit (*a searcher*, figure 4, element 18) comprising a correlator (figure 4, comprising elements 205 and

206) correlating received signals (*a first signal*) with pilot spreading codes and inputting outputs from a de-spreader to a phase rotator (*a correlator configured to produce a plurality of first correlated values, comprising a partial coherent sum, from first signal and second signals*), a transformer (*a processor*, figure 4, comprising elements 169 and 19) taking correlated samples (*a plurality of first correlated values)* from the correlator and transforming to a frequency domain signal from a time domain signal (*second correlated values)* (*a processor configured to transform the first correlated values into a plurality of second correlation values related to a different frequency component of the first signal*), and a detector (figure 4, element 170) to monitor the second correlation values over a time period and select one of the frequency components having a peak second correlation value (column 7, line 66 to column 8, line 8). Furukawa discloses monitoring correlation values over a time period to select a peak correlation value (figure 4, element 170). Furukawa discloses a multiplier multiplying the first signal portion (I and Q signal) with the second signal PN(I) and PN(Q) to produce a plurality of product values (figure 4), but fails to disclose the multiplier comprising 96 multipliers each producing one product value. Yamada discloses adders producing three coherent sums (figure 2, element 26; column 6, lines 21-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Brunner to implement a multiplier comprising 96 multipliers, as suggested by Yamada, for the benefit of preventing the received signal from becoming degraded.

Re claims 27, 28, 77 and 78, Furukawa discloses a delay device with 64 chip delay (*a buffer with a shift register*, figure 6, element 70) providing a first signal to the multiplier (figure 6, element 80).

Re claims 29 and 79, Furukawa discloses a delay device with 64 chip delay (*a buffer with a shift register*, figure 6, element 70) providing a first signal to the multiplier (figure 6, element 80).

Re claims 30, 31, 80 and 81, Furukawa inherently discloses a delay device receiving chips and providing a chip to the multiplier.

Re claims 33 and 83, Furukawa and Yamada disclose producing three coherent sums by combining three delayed signals with optimum weights, but fail to disclose combining three different product value portions each comprising 32 product values. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Furukawa and Yamada to combine three product value portions for the benefit of preventing the received signal from becoming degraded.

Claims 6 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brunner in view of Yamada and further in view of Sakoda (US 6909704).

Re claims 6 and 56, Brunner and Yamada disclose all of the limitations of the base claim, but fail to disclose the portion of the first signal and the second signal each comprising 96 chips. Sakoda discloses a pilot interval to be 96 chips (column 1, lines 42-43). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the chip rate of Brunner and Yamada to be 96 so that the

chip rate for transmitting a pilot signal would be distinguished from that of a power control signal.

Claims 34-36, 84 and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa in view of Yamada and further in view of Brunner.

Re claims 34-36, 84 and 85, Furukawa and Yamada disclose all of the limitations of the base claim, but fail to disclose the processor being a discrete or fast Fourier transform. Brunner discloses the frequency device being a discrete Fourier transformer or a fast transformer (column 4, lines 24-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the orthogonal transformation function by fast Hadamard transform with fast Fourier transform since fast Fourier transform is commonly used technique for orthogonal transformation.

Allowable Subject Matter

4. Claims 38-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 14-21, 23, 41-46, 49, 50, 64-71 and 73 are allowed.

Response to Arguments

6. Applicant's arguments filed on 08/17/2007 have been fully considered but are not persuasive.

On page 15 of the Remarks, the applicant argues that Yamada does not disclose producing a plurality of coherent sums each comprising one of the first correlation values by stating that Yamada discloses a single adder for producing a single output. The examiner respectfully disagrees. Yamada discloses adders producing three coherent sums (figure 2, element 26; column 6, lines 21-23). Therefore the rejection of claims stands.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Cho whose telephone number is 571-272-3087. The examiner can normally be reached on Mon-Fri during 7 am to 4 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WING CHAN 9/28/07
SUPERVISORY PATENT EXAMINER

he
Hong Cho
Patent Examiner
9/19/07